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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,596	06/25/2003	Wataru Saito	239400US2S	1453
22850	7590 11/30/2004		EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.			OWENS, DOUGLAS W	
1940 DUKE S ALEXANDR	IA, VA 22314		ART UNIT	PAPER NUMBER
			2811	
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DATE MAILED: 11/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

1		D,	
	Application No.	Applicant(s)	<i></i>
Officia Action Communication	10/602,596	SAITO ET AL.	
Office Action Summary	Examiner	Art Unit	··
	Douglas W Owens	2811	
The MAILING DATE of this communication a Period for Reply	ppears on the cover sheet w	th the correspondence address	
A SHORTENED STATUTORY PERIOD FOR REF THE MAILING DATE OF THIS COMMUNICATION  - Extensions of time may be available under the provisions of 37 CFR after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a r  - If NO period for reply is specified above, the maximum statutory perions  - Failure to reply within the set or extended period for reply will, by state than three months after the material patent term adjustment. See 37 CFR 1.704(b).	N. 1.136(a). In no event, however, may a reply within the statutory minimum of thir od will apply and will expire SIX (6) MON tute, cause the application to become Al	reply be timely filed  ty (30) days will be considered timely.  ITHS from the mailing date of this communication.  BANDONED (35 U.S.C. § 133).	
Status			
1) Responsive to communication(s) filed on 23	August 2004.		
2a)⊠ This action is <b>FINAL</b> . 2b)□ TI	his action is non-final.		•
3) Since this application is in condition for allow	vance except for formal mat	ers, prosecution as to the merits is	
closed in accordance with the practice unde	r <i>Ex parte Quayle</i> , 1935 C.E	). 11, 453 O.G. 213.	
Disposition of Claims			
4)⊠ Claim(s) <u>1-4,6-28</u> is/are pending in the appli	cation.		
4a) Of the above claim(s) is/are withd	rawn from consideration.		
5)⊠ Claim(s) <u>22,26 and 27</u> is/are allowed.			
6)⊠ Claim(s) <u>1-4,6,7,9-15,21,23-25</u> is/are rejecte	ed.		
7) $\boxtimes$ Claim(s) <u>8,16-20 and 28</u> is/are objected to.			
8) Claim(s) are subject to restriction and	d/or election requirement.		
Application Papers			
9)☐ The specification is objected to by the Exami			
10) The drawing(s) filed on is/are: a) a	ccepted or b) ☐ objected to	by the Examiner.	
Applicant may not request that any objection to the	he drawing(s) be held in abeyar	ice. See 37 CFR 1.85(a).	
Replacement drawing sheet(s) including the corr	•		
11) ☐ The oath or declaration is objected to by the	Examiner. Note the attached	d Office Action or form PTO-152.	
Priority under 35 U.S.C. § 119		,	
12) Acknowledgment is made of a claim for forei  a) All b) Some * c) None of:		3 119(a)-(d) or (f).	<u>.</u>
<ul><li>1. Certified copies of the priority docume</li><li>2. Certified copies of the priority docume</li></ul>		unnlication No	
<ul><li>2. Certified copies of the priority docume</li><li>3. Copies of the certified copies of the priority docume</li></ul>			
application from the International Bure	•	received in this National Stage	
* See the attached detailed Office action for a li		received.	
Attachment(s)			
1) Notice of References Cited (PTO-892)		Summary (PTO-413)	
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)		s)/Mail Date nformal Patent Application (PTO-152)	
<ol> <li>Information Disclosure Statement(s) (PTO-1449 or PTO/SB/0 Paper No(s)/Mail Date</li> </ol>	6) Other:		

Application/Control Number: 10/602,596 Page 2

Art Unit: 2811

## **DETAILED ACTION**

# Claim Objections

1. Claim 28 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The claim is a near replica of claim 27, from which claim 28 depends.

# Claim Rejections - 35 USC § 112

- 2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

  The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
- 3. Claims 21 and 23 25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 21 recites the limitation, "wherein insulating film are interposed every border regions between the second semiconductor layer and the third semiconductor layers." The scope of the claim is not clear because it is not clear what is intended by the term "border regions". Additionally, the language used in this limitation makes the scope of the claim difficult to understand.

# Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

Art Unit: 2811

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1 – 4, 6, 7, 9 – 15 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,693,338 to Saitoh et al.

Regarding claims 1 and 21, Saitoh et al. teach a power semiconductor device (Fig. 2, for example), comprising:

a first semiconductor layer (11) of the first conductivity type;

a second semiconductor layer (19) of the first conductivity type and a third semiconductor layer (18) of a second conductivity type which are alternately and laterally arranged on the first semiconductor layer;

a first main electrode (16) in electrical contact with the first semiconductor layer;

a fourth semiconductor layer (12) of the second conductivity type selectively formed in surface regions of the second and third semiconductor layers;

a fifth semiconductor layer (13) of the first conductivity type selectively formed in a surface region of the fourth semiconductor layer;

a second main electrode (17) formed in contact with surfaces of the fourth and fifth semiconductor layers; and

a control electrode (15) formed on surfaces of the second, fourth and fifth semiconductor layers,

wherein an insulating material (22) is interposed between the second and third semiconductor layers in the border regions, where the border regions are taken to be the regions located on the left of the third layer (18); and

wherein an impurity concentration of the first semiconductor layer is lower than that of the second semiconductor layer (Col. 8, lines 9 - 20; Col. 10, lines 26 - 30) and a layer thickness ratio A is given by an expression:

$$0 \ A = t/(t+d) \le 0.72 \ (Col. 8, lines 5 - 7)$$

where t is a thickness of the first semiconductor layer, and d is a thickness of the second semiconductor layer; and

wherein assuming that a breakdown voltage is represented by VB, then VB, t, B and A satisfy the relationship,

 $t < 2.53 \times 10^{-6} \times (A \times VB)^{7/6}$  (cm), since the device disclosed by Saitoh et al. is identical to that of the instant application. For example, t (first semiconductor layer, 11) can be selected to be 15 microns, and d (second semiconductor layer, 19) can be 7 microns, which would result in a ratio of 0.68. The ratio would be within the desired ratio discussed in lines 2-7 of column 8, and shown graphically in Fig. 3A. The range of thicknesses that would result in a functioning device, while maintaining the desired range, is considered to be disclosed inherently by Saitoh et al., just as it is considered to be disclosed in the instant application, which does not explicitly disclose all possible combinations of thicknesses. The proposed values would result in the expression, 2.53  $\times 10^{-6} \times (A \times VB)^{7/6}$  (cm) being equal to about 28.2, which is greater than the thickness t, of 15 microns.

Art Unit: 2811

Regarding claim 2, Saitoh et al. teach a semiconductor device, wherein, assuming an aspect ration B is represented by B = d/w (d = 7 microns, for example), where w is an interval between adjacent third semiconductor layers (w = 8 microns, for example; Col 8, lines 20 - 21), the layer thickness ratio A (A = 0.68, for example; discussed above) and the aspect ratio B (B = 0.87) satisfy an expression below:

 $A \times B \le 1.15$ ,

since  $A \times B = 0.596$ .

Regarding claim 3, Saitoh et al. teach a semiconductor device, wherein an aspect ration B and the layer thickness ration A satisfy an expression below:

$$-0.04B + 0.48 < (A \times B) < 0.13B + 0.59.$$

since 0.445 (left term) is less than 0.596 (middle term), which is less than 0.704 (right term).

Regarding claim 4, Saitoh et al. teach a device, wherein A x B satisfies the relationship:

$$0.58 < (A \times B) < 0.71$$
, where A = 0.68, for example.

Regarding claim 6, Saitoh et al. inherently teach a device, wherein Nn, VB and A satisfy the relationship,

Nn > 1.11 x  $10^{18}$  x (A x  $\overline{VB}$ )  $^{4/3}$  ( $\overline{cm}^{-3}$ ), since the device disclosed by Saitoh et al. is identical to that of the instant application. Moreover, Saitoh et al. teach the optimal impurity concentration of the first semiconductor layer, as disclosed on page 17 of the instant application, in lines 10 and 11 of column 8.

Regarding claim 7, Saitoh et al. teach a device (Fig. 6), wherein an insulating material (22) is interposed between the second and third semiconductor layers.

Regarding claims 9 – 15, Saitoh et al. teach a device, wherein an impurity concentration profile at least one of the second semiconductor layer and third semiconductor layer reduces with depth. This feature is shown in Fig. 4c, where the impurity concentration gradually reduces near the junction with the first semiconductor.

# Allowable Subject Matter

- 6. Claims 8, 16 20 and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
- 7. Claims 22, 26 and 27 are allowed.
- 8. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record does not teach, alone or in combination, a power device, "wherein a void is present in a border region between the second semiconductor layer and the third semiconductor layer."

#### Response to Arguments

9. Applicant's arguments filed August 23, 2004 have been fully considered but they are not persuasive.

Applicant argues that Saitoh et al. do not teach an embodiment that satisfies the expressions,  $0 \le A = t/(t+d) \le 0.72$  and  $t \le 2.53 \times 10^{-6} \times (A \times VB)^{7/6}$  (cm). The crux of the disclosure of Saitoh et al. is to form a device, wherein the ratio of the first layer to the sum of the first and second layer remains within a specific range (See, Fig. 3A for

Art Unit: 2811

example) for the purpose of reducing on resistance. For example, t (first semiconductor layer, 11) can be selected to be 15 microns, and d (second semiconductor layer, 19) can be 7 microns, which would result in a ratio of 0.68. The ratio would be within the desired ratio discussed in lines 2 – 7 of column 8, and shown graphically in Fig. 3A. The range of thicknesses that would result in a functioning device, while maintaining the desired range, is considered to be disclosed inherently by Saitoh et al., just as it is considered to be disclosed in the instant application, which does not explicitly disclose all possible combinations of thicknesses. The instant application only cites specific thicknesses of t=14.1, and the ratio B being equal to 2, which would require d to be 16. In the cited example, the expression  $-0.04B + 0.48 < (A \times B) < 0.13B + 0.59$  is not satisfied, since the right side of the inequality is 0.85, which is less that A x B (0.94). However, the application is interpreted from the viewpoint of one having ordinary skill in the art. Accordingly, the disclosure is enabling and the appropriate thicknesses are considered to be disclosed. The proposed values would result in the expression, 2.53 x 10<sup>-6</sup> x (A x VB)<sup>7/6</sup> (cm) being equal to about 28.2, which is greater than the thickness t, of 15 microns.

Applicant argues that Saitoh et al. do not disclose an insulating film interposed at every-border region between the second and third semiconductor layers. This teaching can be seen in Figure 6, wherein the border region is taken to be the area on the left of the third semiconductor layer.

Application/Control Number: 10/602,596 Page 8

Art Unit: 2811

## Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W Owens whose telephone number is 571-272-1662. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Application/Control Number: 10/602,596

Art Unit: 2811

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Page 9

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